FORM PTO-1390 (Modified) (REV 11-2000) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER: 211601US2PCT

U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR): 09/889558

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/FR00/00198	28 JANUARY 2000	29 JANUARY 1999

TITLE OF INVENTION

DEVICE FOR PROTECTION AGAINST ELECTROSTATIC DISCHARGES FOR MICROELECTRONIC COMPONENTS ON SOI TYPE SUBSTRATE

APPLICANT(S) FOR DO/EO/US

Charles LEROUX

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include itens (5), (6), (9) and (24) indicated below.
4. ☒ The US has been elected by the expiration of 19 months from the priority date (Article 31).
5. ☒ A copy of the International Application as filed (35 U.S.C. 371 (c) (2))
   a. ☐ is attached hereto (required only if not communicated by the International Bureau).
   b. ☒ has been communicated by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☒ An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. ☒ is attached hereto.
   b. ☐ has been previously submitted under 35 U.S.C. 154(d)(4).
7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371 (c)(3))
   a. ☐ are attached hereto (required only if not communicated by the International Bureau).
   b. ☐ have been communicated by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.
8. ☐ An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371 (c)(4)).
10. ☒ An English language translation of the annexes of the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).
11. ☐ A copy of the International Preliminary Examination Report (PCT/IPEA/409).
12. ☒ A copy of the International Search Report (PCT/ISA/210).

Items 13 to 20 below concern document(s) or information included:

13. ☐ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
14. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
15. ☒ A **FIRST** preliminary amendment.
16. ☐ A **SECOND** or **SUBSEQUENT** preliminary amendment.
17. ☐ A substitute specification.
18. ☐ A change of power of attorney and/or address letter.
19. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821 - 1.825.
20. ☐ A second copy of the published international application under 35 U.S.C. 154(d)(4).
21. ☐ A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
22. ☐ Certificate of Mailing by Express Mail
23. ☒ Other items or information:

Request for Consideration of Documents in International Search Report
Notice of Priority / PCT/IB/304 / PCT/IB/308
Drawings (3 sheets) / Amended Sheets (pages 19, 20 & 21)

U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR)	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
09/889558	PCT/FR00/00198	211601US2PCT

24. The following fees are submitted:	CALCULATIONS PTO USE ONLY
BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)) :	
☐ Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO **$1000.00**	
☒ International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO **$860.00**	
☐ International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO **$710.00**	
☐ International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4) **$690.00**	
☐ International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4) **$100.00**	
ENTER APPROPRIATE BASIC FEE AMOUNT =	**$860.00**
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (e)).	**$0.00**

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE	
Total claims	10 - 20 =	0	x $18.00	**$0.00**
Independent claims	3 - 3 =	0	x $80.00	**$0.00**
Multiple Dependent Claims **(check if applicable).**			☐	**$0.00**

TOTAL OF ABOVE CALCULATIONS =	**$860.00**
☐ Applicant claims small entity status. (See 37 CFR 1.27). The fees indicated above are reduced by 1/2.	**$0.00**
SUBTOTAL =	**$860.00**
Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (f)). +	**$0.00**
TOTAL NATIONAL FEE =	**$860.00**
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31) **(check if applicable).** ☐	**$0.00**
TOTAL FEES ENCLOSED =	**$860.00**
Amount to be: refunded	$
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a. ☒ A check in the amount of **$860.00** to cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account No. _____ in the amount of _____ to cover the above fees. A duplicate copy of this sheet is enclosed.

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NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

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REGISTRATION NUMBER

7-27-01
DATE

211601US

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF :

CHARLES LEROUX : ATTN: APPLICATION DIVISION

SERIAL NO: NEW U.S. PCT APPLN :
(Based on PCT/FR00/00198)

FILED: HEREWITH :

FOR: DEVICE FOR PROTECTION AGAINST ELECTROSTATIC DISCHARGES FOR MICROELECTRONIC COMPONENTS ON SOI TYPE SUBSTRATE :

PRELIMINARY AMENDMENT

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

Prior to a first examination on the merits, please amend the above-identified application as follows:

IN THE CLAIMS

Please cancel Claims 1-10 without prejudice.

Please add new Claims 11-20 as follows:

11. (New) Device for protection of an electronic component against electrostatic discharges, the device being made in a semiconducting layer of a substrate, the semiconducting layer covering an insulating layer, the device being connected to a contact

pin to protect the component in order to divert an electrostatic discharge, the device comprising at least one Zener diode connected to the contact pin to be directly polarized.

12. (New) Device according to claim 11, further comprising plural Zener diodes mounted in series and connected to the contact pin to be directly polarized.

13. (New) Device according to claim 11, wherein the at least one Zener diode comprises two regions strongly doped with opposite conductivity types, the two regions being separated by a region doped to an average level according to either of the conductivity types.

14. (New) Device according to claim 13, wherein the semiconducting layer of the substrate is a silicon layer, the doping of the two regions with strong doping being of the order of 10^{20} atoms/cm^3, the doping of the region with medium level doping being of the order of 10^{18} atoms/cm^3.

15. (New) Device according to claim 11, wherein the said substrate is an SOI substrate.

16. (New) Device according to claim 12, wherein the plural the Zener diodes are laid out adjacent to each other to form a series installation, an electrical link between two adjacent Zener diodes being obtained by a metallization.

17. (New) Device according to claim 12, wherein the plural Zener diodes are laid out adjacent to each other to form a series installation, an electrical link between two adjacent Zener diodes being obtained by a silicide.

18. (New) Method for making a device for protection of an electronic component against electrostatic discharges, the protection device comprising at least one Zener diode made in a semiconducting layer of a substrate, the semiconducting layer covering an insulating layer, the method comprising:

a step to define a zone of the diode or an active zone, in the semiconducting layer,

a step to implant a first zone in the active zone, to obtain the first zone with medium doping according to a conductivity type chosen between a first conductivity type and a second conductivity type opposite to the first conductivity type,

a step to implant a part of the first zone, to obtain a second strongly doped zone according to the first conductivity type, the second zone being separated from an unimplanted part of the active zone by a remaining part of the first zone, and

a step to implant the unimplanted part of the active zone to obtain a third zone with strong doping according to the said second conductivity type.

19. (New) Method for making a device for the protection of an electronic component against electrostatic discharges, the protection device comprising at least one Zener diode made in a semiconducting layer of a substrate, the semiconducting layer covering an insulating layer, the method comprising:

a step to define a zone of the diode or an active zone in the semiconducting layer,

a step to implant a first zone near a central part of the active zone, to obtain a first medium doped zone according to a conductivity type chosen between a first conductivity type and a second conductivity type opposite to the first conductivity type,

a step to form a grid made of a conducting material on the first zone, after formation of a thin grid oxide layer,

a step to implant a second zone of the active zone adjacent to the first zone, to obtain a second zone with strong doping according to the first conductivity type,

a step to implant a third zone in the active zone, adjacent to the first zone that separates it from the second zone, to obtain a third zone with strong doping according to the second conductivity type.

20. (New) Method according to claim 19, wherein the first zone is wider than the grid formed on the first zone.

IN THE ABSTRACT OF THE DISCLOSURE

Please delete the original Abstract page 22 in its entirety and insert therefor:

ABSTRACT OF THE DISCLOSURE

A device for the protection of an electronic component against electrostatic discharges. The device is made in a semiconducting layer of a substrate. The semiconducting layer covers an insulating layer. The device is connected to a contact pin to protect the electric component in order to divert an electrostatic discharge. The device includes at least one Zener diode connected to the pin to be directly polarized.

REMARKS

Favorable consideration of this application, as presently amended, is respectfully requested.

The present Preliminary Amendment is submitted to place the above-identified application in more proper format under United States practice. By the present Preliminary Amendment original claims 1-10 are canceled and new claims 11-20 are presented for examination. New claims 11-20 are deemed to be self-evident from the original disclosure, including original claims 1-9, and thus are not deemed to present any issues of new matter. A

new Abstract believed to be in more proper format under United States practice is also submitted herein.

The present application is believed to be in condition for a full and thorough examination on the merits. An early and favorable consideration of the present application is hereby respectfully requested.

Respectfully submitted,

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211601US

Marked-Up Copy
Serial No:

Amendment Filed on:
07-27-01

IN THE CLAIMS

--Claims 1-10 (Canceled).

Claims 11-20 (New).--

IN THE ABSTRACT OF THE DISCLOSURE

Please delete the original Abstract page 22 in its entirety and insert therefor:

ABSTRACT OF THE DISCLOSURE

[The invention relates to] A device [(25)] for the protection of an electronic component against electrostatic [discharges,] discharges. [the] The device [(25) being] is made in a semiconducting layer of a [substrate,] substrate. [the] The semiconducting layer [covering] covers an insulating [layer,] layer. [the] The device [being] is connected to a contact pin [(21 to 24)] to protect the [said] component in order to divert an electrostatic [discharge, characterized in that the] discharge. The device [(25) comprises] includes at least one Zener diode connected to the [said] pin to be directly polarized.

[Fig. 4]

DEVICE FOR PROTECTION AGAINST ELECTROSTATIC DISCHARGES FOR MICROELECTRONIC COMPONENTS ON SOI TYPE SUBSTRATE

Technical field

This invention relates to a device for protection against electrostatic discharges for electronic components made on a substrate comprising a semiconducting layer on an insulating layer, for example an SOI substrate.

Protection against electrostatic discharges (ESD) has an important influence on the reliability of electronic systems. According to some sources, losses caused by electrostatic discharges account for an average loss of products varying between 8 and 33%. Protection against these nuisances is necessary at all levels; manufacturing and operating environment of integrated circuits, protection on cards combining several integrated circuits. Part of the protection is provided by the circuit itself.

The various integrated circuits used in electronic systems are connected to their environment through their input-output or power supply pins, and therefore if an electrostatic discharge (ESD) occurs, it can be passed through these pins. The main principle for protection on the circuit is then to put protection structures between these pins and their power supplies at each input-output pin around the periphery of the circuit. These protective structures are usually inverse diodes, blocked MOS transistors or thyristors. These devices must not disturb operation of the circuit and must behave like open switches during normal

operation in order to directly divert the minimum amount of input-output current that forms the vector for carrying information in the circuit, to the circuit power supplies. On the other hand when a discharge occurs, they must behave like closed switches to prevent the electrostatic discharge from degrading the internal part of the circuit. If a discharge occurs, and if the protection really operates like an ideal switch, in other words a zero resistance series switch, the electrostatic discharge will flow through the circuit without any loss of energy and therefore without deterioration. The electrostatic discharge voltage resisted by the protection device without being damaged is called the intrinsic withstand.

State of prior art

The switch analogy is an ideal case, and an attempt will be made to approach this ideal case. In practice, protection is characterized by its electrical characteristic hold voltage in triggered mode and its resistance in series. Therefore, optimising protection means minimizing the size of the structure, with a minimum resistance in series and for which the hold voltage is minimized, although remaining greater than the circuit operating voltage. The reduction in the surface area occupied by the protection structure and the reduction in its resistance are usually contradictory, and a compromise has to be reached between these two factors.

At the present time, integrated circuits operating at increasing low voltages (less than 3 V and even less

than 2 V) can now be made. The maximum allowable voltages are also lower and optimisation of the series resistance of protection structures, and achieving an optimum hold voltage become essential challenges.

Protection structures using several directly polarized diodes have been used within this context of protection of low voltage circuits. The hold voltage is defined as a first approximation by the diode elbow voltage (about 0.7 V) multiplied by the number of diodes in series.

The use of this type of protection by diodes in series creates difficulties on a classical silicon substrate due to the fact of a parasite effect commonly called the Darlington effect. On this type of substrate, each protection diode is made in a compartment with doping type opposite to the doping type of the substrate, each compartment being isolated from the others, the diodes then being connected in series. Since the substrate is solid, a parasite bipole transistor is connected to each protection diode. The protection diode leakage current corresponds to the basic current of the transistor connected to the next protection diode and the leakage current is correspondingly amplified. Document WO 97/35373 proposes a solution to this problem by decorrelating the isolation and protection functions. The Darlington effect is used to perform the electrostatic discharge evacuation function. The size of the first diode is maximized since the first diode receives the largest part of the discharge. The isolation function is then

performed by a MOS transistor connected in series with the last protection diode.

The Darlington effect does not occur in microelectronic circuits made on SOI (silicon on insulator) substrates since parasite bipole transistors are eliminated. Protection by diodes in series can therefore be applied on these substrates.

The article entitled "Dynamic Threshold Body-and Gate-Coupled SOI ESD Protection Networks" by S. VOLDMAN et al. published in EOS/ESD Symposium proceedings, 1997, Santa Clara, California, pages 210-220, divulges a protection device using diodes made on an SOI substrate. The protection diodes are then made from MOS transistors. For such a transistor made on SOI substrate, the area under the grid causes a problem due to the fact that the buried insulating layer prevents dissipation of heat, which is contrary to what happens for a solid silicon substrate. This article emphasizes protections in which the diode is made between firstly the drain, substrate and grid, and secondly the source. However, the most compact useable diode consists of an NMOS transistor with a different type of source implant and drain implant. Some manufacturing techniques require a small thickness of silicon on the buried oxide layer, and the formed diodes then have a high resistance. The area under the grid of a protection diode can melt when an electrostatic discharge occurs, since the heat produced cannot easily be dissipated.

Presentation of the invention

The invention provides a solution to the problem of protecting microelectronic circuits produced on SOI type substrates. It is applicable to the very particular context of low consumption integrated circuits. The general principle of the invention is to use a device which also has very bad inverse withstand performances and cannot be used in a circuit without modification due to the leaks that it causes. This device is a Zener type diode. This term refers to a diode with a low avalanche voltage. Its bad inverse withstand is not a disadvantage in the case of the invention, since the diode will always be directly polarized.

The Zener diode used according to this invention is a diode formed by the junction between two opposite and highly doped zones. The direct characteristics and the inverse characteristics are correspondingly degraded and the result is that the diode cannot be used in an application for which this type of diode is usually used. Its conduction level at a given voltage is then increased, while its blocking aspect when inversely polarized disappears. Leaks with low polarization voltage are also higher than with a classical diode.

The advantage of Zener diodes is that their intrinsic voltage withstand at an electrostatic discharge is high. This is particularly true in the case of a thin substrate (see FIGURE 7). Furthermore they have a lower series resistance and their gain is

increased by a factor of 3. These two parameters are essential to optimise protection.

Therefore, the purpose of the invention is a device for protection of an electronic component against electrostatic discharges, the device being made in a semiconducting layer of a substrate, the semiconducting layer covering an insulating layer, the device being connected to a contact pin to protect the said component in order to divert an electrostatic discharge, characterized in that the device comprises at least one Zener diode connected to the said pin to be directly polarized.

In general, this device comprises several Zener diodes mounted in series and connected to the said pin to be directly polarized. The Zener diodes may be laid out adjacent to each other to form the circuit in series, the electric link between two adjacent diodes being obtained by metallisation or by a silicide.

Advantageously, each Zener diode comprises two regions highly doped with opposite types of conductivity, these two regions being separated by a medium doping region according to one or the other of the said types of conductivity. Preferably, if the semiconducting substrate layer is a silicon layer, the doping levels in the two strongly doped regions is of the order of 10^{20} atoms/cm^3, and the doping level in the region doped at an average level is of the order of 10^{18} atoms/cm^3. This substrate may be an SOI substrate.

In order to overcome the problem of dissipation of heat from a protection diode made on a semiconducting

surface layer supported on an insulating layer that is a poor dissipator of heat (for example an SOI substrate), it is proposed to make this diode without starting from a transistor to avoid the presence of a grid, in order to obtain the greatest volume and thus enable dispersion of heat. The silicon will be thinned if necessary at the grid.

Another purpose of the invention is a process for embodiment of a device for protection of an electronic component against electrostatic discharges, the protection device comprising at least one Zener diode made in a semiconducting layer of a substrate, the semiconducting layer covering an insulating layer, the process comprising:

- a step to define the zone of the diode or the active zone, in the said semiconducting layer,
- a step to implant a first zone in the said active zone, to obtain a first zone with medium doping according to a conductivity type chosen between a first conductivity type and a second conductivity type opposite to the first conductivity type,
- a step to implant a part of the said first zone, to obtain a second strongly doped zone according to the said first conductivity type, the second zone being separated from the unimplanted part of the active zone by the remaining part of the first zone,
- a step to implant the unimplanted part of the active zone to obtain a third zone with strong doping according to the said second conductivity type.

Another purpose of the invention is a process for making a device for the protection of an electronic

component against electrostatic discharges, the protection device comprising at least one Zener diode made in a semiconducting layer of a substrate, the semiconducting layer covering an insulating layer, the process comprising:

- a step to define the zone of the diode or the active zone in the said semiconducting layer,
- a step to implant a first zone near the central part of the active zone, to obtain a first medium doped zone according to a conductivity type chosen between a first conductivity type and a second conductivity type opposite to the first conductivity type,
- a step to form a grid made of a conducting material on the first zone, after formation of a thin grid oxide layer,
- a step to implant a second zone of the active zone adjacent to the first zone, to obtain a second zone with strong doping according to the first conductivity type,
- a step to implant a third zone in the active zone, adjacent to the first zone that separates it from the second zone, to obtain a third zone with strong doping according to the second conductivity type.

Preferably, the first zone is wider than the grid formed on this first zone.

Brief description of the drawings

The invention will be better understood and other advantages and specific features will appear after reading the following description, given as a non-

limitative example accompanied by the attached drawings, among which:

- FIGURE 1 diagrammatically shows the composition of a Zener diode that can be used in the protection device according to the invention;

- FIGURE 2 is a descriptive view of the implant of a Zener diode on a very thin substrate layer that can be used in the protection device according to the invention;

- FIGURE 3 is a descriptive view of the implant of a Zener diode on a thin layer of a substrate that can be used in the protection device according to the invention;

- FIGURE 4 represents an electronic circuit protected by protection devices according to the invention;

- FIGURE 5 represents the implant of a set of four Zener diodes mounted in series on a very thin layer of a substrate, for a protection device according to the invention;

- FIGURE 6 represents the implant of a set of four Zener diodes mounted in series on a thin layer of a substrate, for a protection device according to the invention;

- FIGURE 7 is a cross sectional view of MOS transistor according to known art;

- FIGURES 8 to 11 are cross sectional views of an SOI substrate during various manufacturing steps of a Zener diode for a protection device according to the invention.

Detailed description of embodiments of the invention

FIGURE 1 diagrammatically shows the composition of a Zener diode that can be used in the protection device according to the invention. This Zener diode is made from single crystalline silicon using two strong source and drain type implants that can be used to achieve doping of the order of 10^{20} atoms/cm^3. These two opposite types of implants, N^{++} for region 1 and P^{++} for region 2, are separated by an intermediate N or P type implant in region 3 of the order of 10^{18} atoms/cm^3. This diode is specific in its design and its low resistance. This Zener diode may be made differently depending on the techniques used.

When a classical diode is made starting from a MOS transistor configuration on a very thin layer of an SOI type substrate, the low intrinsic withstand of the protection diode is explained partly by the lower thickness of silicon due to local thinning. Furthermore, zones with the lowest doping located under spacers can induce a high series resistance of the diode, particularly for implants corresponding to the PMOS transistor.

It is proposed that each Zener diode in the protection device according to the invention should be made as follows, in order to overcome these disadvantages. The polysilicon grid masking level is not used. The implant level used for spacers in the NMOS transistor (slightly doped N or LDDN drain) is dissociated from the N drain and source (DSN) level. The P source drain (DSP) level that is normally the

complement of the DSN level, becomes the complement of the DSN and LDDN levels.

FIGURE 2 shows a descriptive view of the implant of a Zener diode on a very thin layer of a substrate. In order to make this diode, an active silicon zone 5 is defined in the silicon surface layer of an SOI substrate. An LDDN type implant level 6, and an N^{++} type implant layer 7 are made. The DSP level is complementary to the DSN and the LDDN levels.

The following table presents the electrical results in terms of ESD withstand and electrical resistance, for a diode according to known art and a Zener diode made using similar techniques and with the same characteristics.

	ESD withstand (volts/µm)	R (Ω)
Diode	7 V/µm	1400 Ω µm
Zener diode	11 V/µm	470 Ω µm

The intrinsic withstand expressed in volts per micrometer, is a value used in the standard test for protection against electrostatic discharges called HBM (for "Human Body Model"). This test was defined by considering that a person can be represented by a capacitor with a capacitance of 100 pF, the skin resistance varying between 500 and 50 000 Ω. This standard refers to a device mounted in series with a 100 pF capacitor, a 1500 Ω resistance and implicitly a 7.5 µH inductance. It is said that a device has a

withstand of 2000 V (HBM) if it is not damaged by the discharge of a capacitor charged to 2000 V, this discharge taking place through the 1500 Ω resistance and the 7.5 µH inductance. The voltage withstand is then normalized per unit width of the protection device.

With this type of tester, and due to the high value of its series resistance which is 1500 Ω, a voltage transient of U volts actually corresponds to a current transient with a maximum current of about U/1500 amperes, a rise time of 5 to 10 nS and an exponential decay with a time constant of 150 nS. This current transient causes a certain temperature rise due to the Joule effect. The ESD withstand in terms of volts per µm corresponds to a limit beyond which the energy dissipated in the device causes a destructive temperature runaway. The temperature runaway threshold may be related to a critical temperature that must not be exceeded. The temperature rise in the material during the ESD transient corresponds to dissipation of heat by the Joule effect together with the high current transient. At the same current densities, the temperature rise for the SOI substrate is greater than for a solid substrate, since heat cannot be dissipated as easily through the back of the substrate due to the presence of the buried oxide layer. The increase in the intrinsic withstand implies an increase in the thickness of the surface silicon layer.

In the above table, the gain in terms of intrinsic withstand and electrical resistance of the diode

according to the invention, is obvious compared with the classical diode.

For another type of technique, namely thin silicon surface layers, local thinning is not used to make a classical diode produced from a classical MOS transistor. In order to overcome resistance problems under the spacer, at least one specific N type implant is used for the purposes of this invention, together with doping of the same order of magnitude as that used for the intermediate zone of the Zener diode, over the entire active zone. This implant creates doping of a few 10^{18} atoms/cm^3 and is done instead of the threshold adjustment implant done for a classical diode.

The implant then used to make the Zener diode according to the invention is shown in FIGURE 3. In order to produce this diode, an active silicon zone 10 is defined in the silicon surface layer of an SOI substrate. An N^{++} type implant level 11, a P^{++} type implant level 12, an N type implant level 13 and a polysilicon grid 14 are made.

The protection device using Zener diodes according to the invention cannot be used in the same way as protection devices with classical diodes. Zener diodes in the protection device according to the invention are polarized directly.

For example, FIGURE 4 shows an electronic circuit protected from electrostatic discharges by four protection devices according to the invention. The ground pin 21, the DC power supply pin 22, the circuit input pin 23 and the circuit output pin 24 are connected to protection devices 25. These protection

devices 25 are formed from four Zener diodes mounted in series and polarized directly. The number of diodes in a device must be sufficient, in order to resist the power supply voltage without inducing an excessive leakage.

The protection device according to the invention may advantageously be completed by the addition of classical inverse polarized diodes at several locations in the circuit in order to increase the efficiency of the protection regardless of the sign of the electrostatic discharge. Thus, references 26 and 27 denote classical diodes installed in addition to some protection devices according to the invention.

Diodes in the protection device shall be mounted in series, consequently it is judicious to design the device to enable the most compact possible integration. This is done by making the four diodes on the same active zone. If the diodes are made using an LDDN level differentiated from the DSN level (see FIGURE 2), these diodes can be connected to each other through the metallisation level. This is illustrated in FIGURE 5. The four diodes 31, 32, 33 and 34 are shown with their different implants, for example for the Zener diode 33, the DSP implant 331, the DSN implant 332 and the LDDN implant 333. Metallisations 35 connect the diodes to each other and to the outside. References 36 represent electrical contact points between diodes and metallisation.

If the diodes were made using an LDDN type level used in front of the grid, then the diodes can be connected by a silicide level as illustrated in

FIGURE 6. The result is an even more highly integrated device. The four diodes are referenced 41, 42, 43 and 44. Each diode, for example diode 43, comprises a DSP implant 431, a DSN implant 432 and a polysilicon grid 433. References 46 represent electrical contact points at the input and output of the protection device with four Zener diodes.

A classical diode is usually made by producing a MOS transistor. FIGURE 7 shows a cross section of such a transistor made on an SOI substrate formed from a solid part 50 made of silicon, a layer of silicon oxide 51 and surface layer of silicon 52. The local thinning area created in the surface layer 52 can be noted. This local thinning area supports the grid oxide layer 53, the polysilicon grid 54 and the spacers 55. Classical diodes are made using this concept and it is obvious that the volume of silicon between the grid oxide 53 and the oxide layer 51 is too confined. The heat produced in this volume cannot easily be dissipated, unlike elements made on the solid silicon substrate.

According to the invention, Zener diodes can be made avoiding local thinning related to the polysilicon grid. The diode is made with a single LDD level as shown in FIGURE 2. This is an innovative modification of a standard process since a device is used which also has very bad inverse withstand performances and which cannot be used as such in a circuit due to the leaks that it causes.

FIGURES 8 to 11 illustrate the production of a Zener diode for a protection device according to the

invention, starting from an SOI substrate. FIGURE 8 shows a cross-section of an SOI substrate composed of a solid part 60 made of silicon, a silicon oxide layer 61 and a silicon surface layer 62. As shown in FIGURE 9, an LDDN type implant is made on part of the surface layer 62 to obtain an N^+ doped zone 63. As shown in FIGURE 10, an N drain-source (DSN) type implant is then made on part of the zone 63 that already has an N^+ type doping. This gives a zone 64 with N^{++} doping. A P drain-source type (DSP) implant is then made in zone 65 in order to complete the Zener diode, as shown in FIGURE 11.

In general, the doping in the different zones forming a Zener diode in the device according to the invention will be greater than or equal to 10^{13} atoms/cm^3.

This Zener diode design is inexpensive, since, although it obviously needs an additional reticle, the LDDN level is dissociated from the DSN level and the resulting production process is not more complex. The protection function is optimised; the intrinsic withstand is increased and the voltage drop developed at the terminals of the protection diode during an electrostatic discharge is minimized. This is shown in the table shown above: 60% gain on the intrinsic withstand and 200% gain on the electrical resistance, which is actually the most critical parameter.

The invention succeeded in reaching a compromise. As doping on the LDD side increases, the avalanche voltage reduces and the direct trip voltage also

reduces. The result is better evacuation of the electrostatic discharge wave.

The isolation capacity reduces as the doping increases. This type of diode made with these non-classical characteristics result in structures that produce high leakage currents but when put in series the isolation capacity is compensated and these diodes are very efficient in evacuating charges.

The invention has the following advantage: when the power supply voltage decreases down to 1 V, the result obtained using two degraded diodes mounted in series provides an excellent protection with low resistance. The inventor of this invention has proved an initial assumption by using a very bad quality of this component.

CLAIMS

1. Device (25) for protection of an electronic component against electrostatic discharges, the device being made in a semiconducting layer (62) of a substrate, the semiconducting layer (62) covering an insulating layer (61), the device (25) being connected to a contact pin (21 to 24) to protect the said component in order to divert an electrostatic discharge, characterized in that the device (25) comprises at least one Zener diode connected to the said pin to be directly polarized.

2. Device according to claim 1, characterized in that it comprises several Zener diodes mounted in series and connected to the said pin to be directly polarized.

3. Device according to one of claims 1 or 2, characterized in that each Zener diode comprises two regions (1, 2) strongly doped with opposite conductivity types, these two regions being separated by a region (3) doped to an average level according to either of the said conductivity types.

4. Device according to claim 3, characterized in that the semiconducting layer of substrate is a silicon layer, the doping of the two regions with strong doping being of the order of 10^{20} atoms/cm^3, the doping of the region with medium level doping being of the order of 10^{18} atoms/cm^3.

English translation of the amended sheets of International Preliminary Examination Report

5. Device according to any one of claims 1 to 4, characterized in that the said substrate is an SOI substrate.

6. Device according to claim 2, characterized in the said the said Zener diodes (31 to 34)are laid out adjacent to each other to form the series installation, the electrical link between two adjacent diodes being obtained by metallisation (35).

7. Device according to claim 2, characterized in that the said Zener diodes (41 to 44) are laid out adjacent to each other to form the series installation, the electrical link between two adjacent diodes being obtained by a silicide.

8. Method for making a device for protection of an electronic component against electrostatic discharges, the protection device comprising at least one Zener diode made in a semiconducting layer of a substrate, the semiconducting layer covering an insulating layer, the method comprising:

- a step to define the zone of the diode or the active zone (5), in the said semiconducting layer,
- a step to implant a first zone (6) in the said active zone (5), to obtain a first zone (6) with medium doping according to a conductivity type chosen between a first conductivity type and a second conductivity type opposite to the first conductivity type,
- a step to implant a part of the said first zone (6), to obtain a second strongly doped zone (7)

according to the said first conductivity type, the second zone (7) being separated from the unimplanted part of the active zone (5) by the remaining part of the first zone,

- a step to implant the unimplanted part of the active zone to obtain a third zone with strong doping according to the said second conductivity type.

9. Method for making a device for the protection of an electronic component against electrostatic discharges, the protection device comprising at least one Zener diode made in a semiconducting layer of a substrate, the semiconducting layer covering an insulating layer, the method comprising:

- a step to define the zone of the diode or the active zone (10) in the said semiconducting layer,

- a step to implant a first zone (13) near the central part of the active zone (10), to obtain a first medium doped zone (13) according to a conductivity type chosen between a first conductivity type and a second conductivity type opposite to the first conductivity type,

- a step to form a grid (14) made of a conducting material on the first zone (13), after formation of a thin grid oxide layer,

- a step to implant a second zone (12) of the active zone (10) adjacent to the first zone (13), to obtain a second zone with strong doping according to the first conductivity type,

- a step to implant a third zone (11) in the active zone (10), adjacent to the first zone (13) that

separates it from the second zone (12), to obtain a third zone (11) with strong doping according to the second conductivity type.

10. Method according to claim 9, characterized in that the first zone (13) is wider than the grid (14) formed on this first zone.

ABSTRACT OF THE DISCLOSURE

DEVICE FOR PROTECTION AGAINST ELECTROSTATIC DISCHARGES FOR MICROELECTRONIC COMPONENTS ON SOI TYPE SUBSTRATE

The invention relates to a device (25) for protection of an electronic component against electrostatic discharges, the device (25) being made in a semiconducting layer of a substrate, the semiconducting layer covering an insulating layer, the device being connected to a contact pin (21 to 24) to protect the said component in order to divert an electrostatic discharge, characterized in that the device (25) comprises at least one Zener diode connected to the said pin to be directly polarized.

Fig. 4

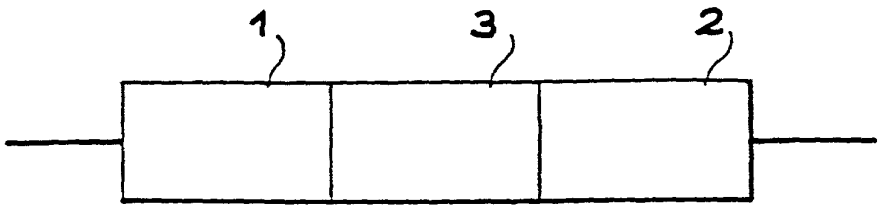

FIG. 1

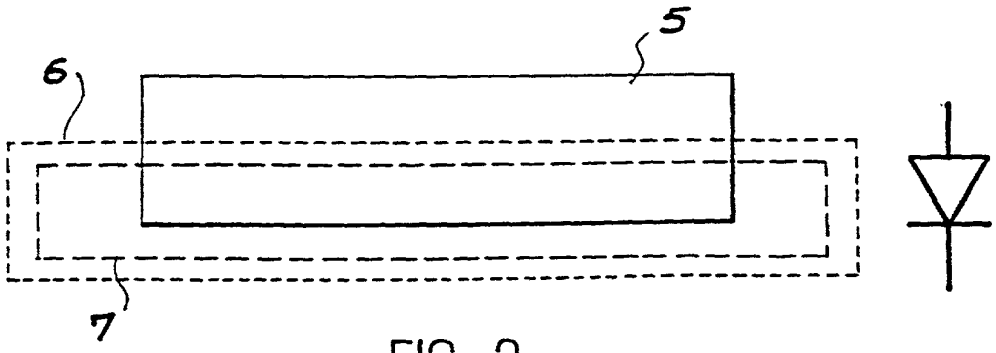

FIG. 2

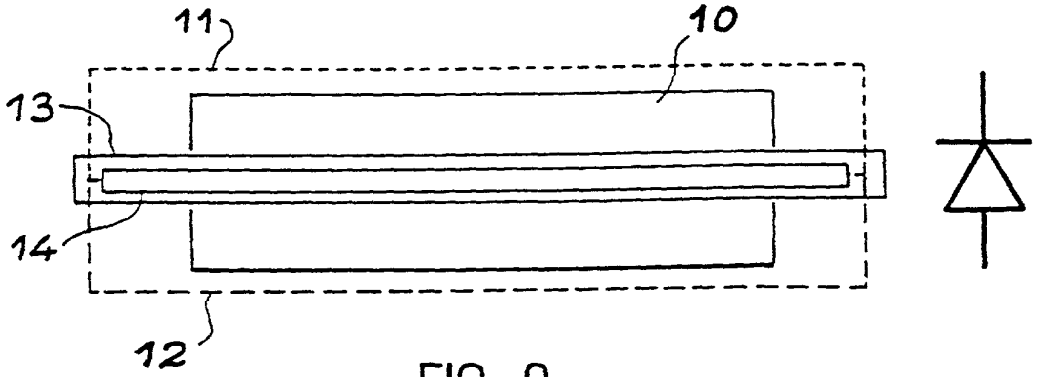

FIG. 3

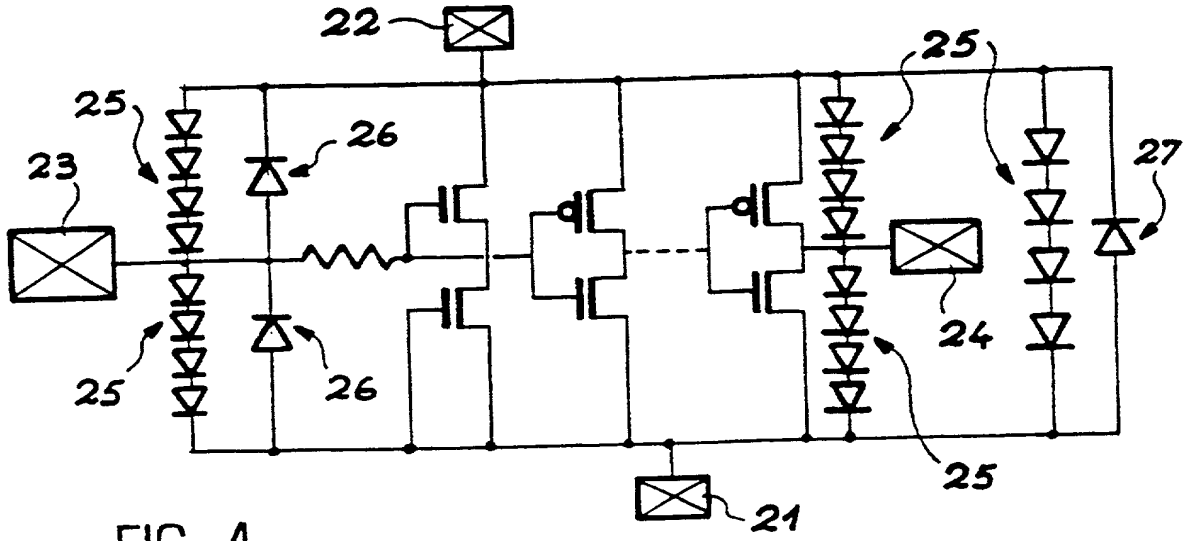

FIG. 4

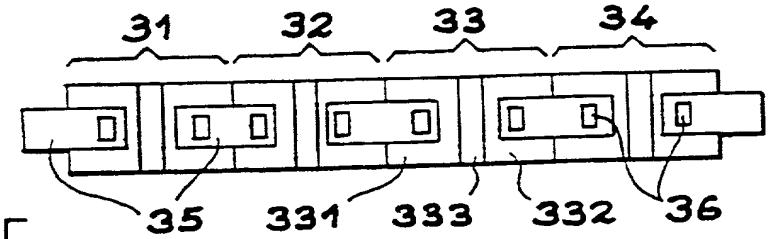

FIG. 5

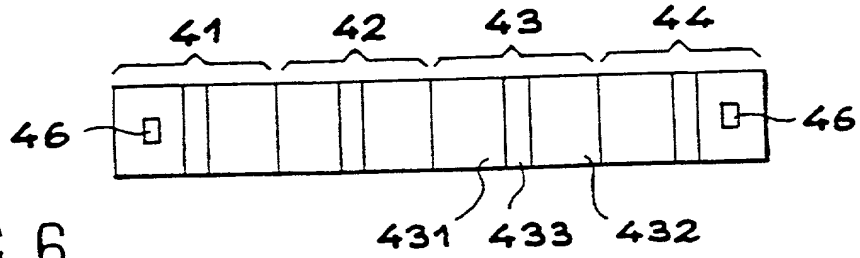

FIG. 6

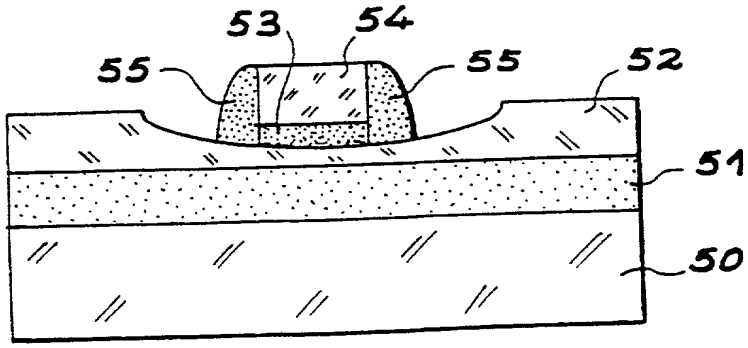

FIG. 7

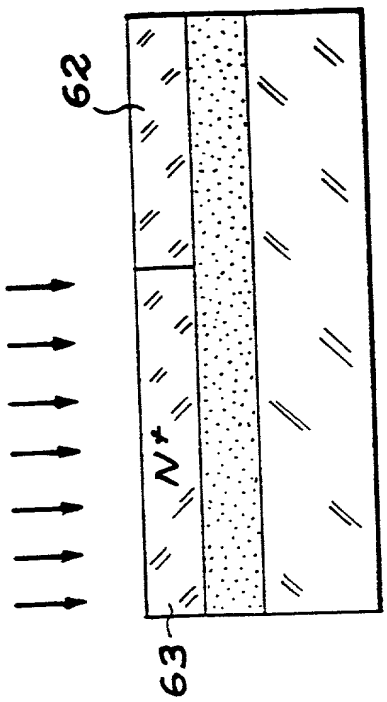

FIG. 9

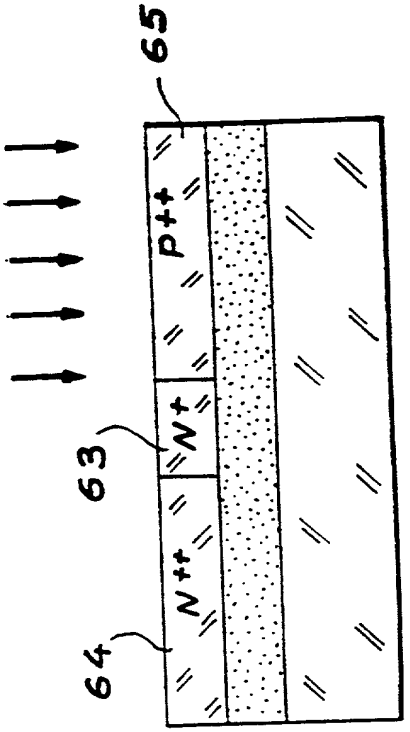

FIG. 11

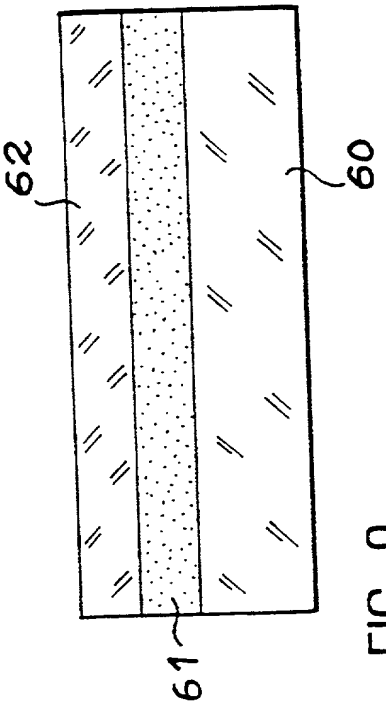

FIG. 8

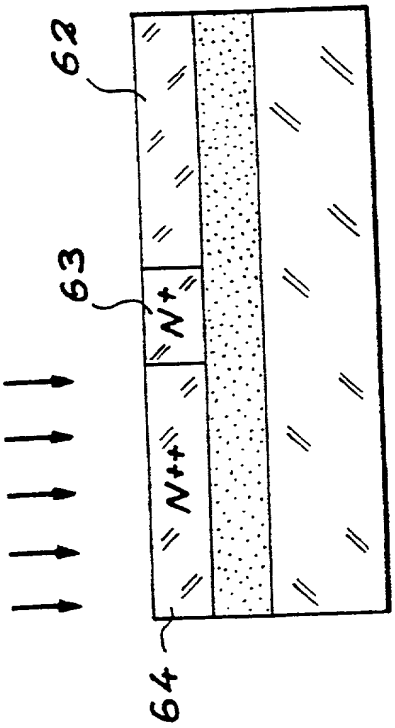

FIG. 10

B 13167.3 JL

Declaration, Power Of Attorney and Petition

WE (I) the undersigned inventor(s), hereby declare(s) that :

My residence, post office address and citizenship are as stated below next to my name,

We (I) believe that we are (I am) the original, first, and joint (sole) inventor(s) of the subject matter which is claimed and for which a patent is sought on the invention entitled

DEVICE FOR PROTECTION AGAINST ELECTROSTATIC DISCHARGES FOR MICROELECTRONIC COMPONENTS ON SOI TYPE SUBSTRATE

the specification of which

☐ is attached hereto.

☐ was filed on

as Application Serial No.

and amended on

☒ was filed as PCT international application

Number PCT/FR00/00198

on January 28, 2000

and was amended under PCT Article 19

on January 17, 2001

We (I) hereby state that we (I) have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

We (I) acknowledge the duty to disclose information known to be material to the patentability of this application as defined in Section 1.56 of Title 37 Code of Federal Regulations.

We (I) hereby claim foreign priority benefits under 35 U.S.C. § 119 (a)-(d) or § 365 (b) of any foreign application(s) for patent or inventor's certificate, or § 365 (a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed. Prior Foreign Application (s)

Application No.	Country	Day/month/Year	Priority Claimed
99 01032	FRANCE	29 JANUARY 1999	☒ YES ☐ NO
			☐ YES ☐ NO
			☐ YES ☐ NO
			☐ YES ☐ NO

We (I) hereby claim the benefit under Title 35, United States Code, § 119 (e) of any United States provisional application(s) listed below.

(Application Number) (Filing Date)

(Application Number) (Filing Date)

We (I) hereby claim the benefit under 35 U.S.C. §120 of any United States application(s), or § 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR § 1.56 which became available between the filing date of prior application and the national or PCT International filing date of this application.

Application Serial No.	Filing Date	Status (pending, patented, abandoned)

And we (I) hereby appoint : Norman F. Oblon, Registration Number 24,618; Marvin J. Spivak, Registration Number 24,913; C, Irvin McClelland, Registration Number 21,214; Gregory J. Maier, Registration Number 25,599; Arthur I. Neustadt, Registration Number 24,854; Richard D. Kelly, Registration Number 27,757; James D. Hamilton, Registration Number 28,421; Eckhard H. Kuesters, Registration Number 28,870; Robert T. Pous, Registration Number 29,099; Charles L. Gholz, Registration Number 26,395; Vincent J. Sunderdick, Registration Number 29,004; William E. Beaumont, Registration Number 30,996; Steven B. Kelber, Registration Number 30,073; Robert F. Gnuse, Registration Number 27,295; Jean-Paul Lavalleye, Registration Number 31,451; William B. Walker, Registration Number 22,498; Timothy R. Schwartz, Registration Number 32,171; Stephen G. Baxter, Registration Number 32,884; Martin M.,. Zoltick, Registration Number 35,745; Robert W. Hahl, Registration Number 33,893; and Richard L. Treanor, Registration Number 36,379; our (my) attorneys, with full powers of substitution and revocation, to prosecute this application and to transact all business in the Patent Office connected therewith; and we (I) hereby request that all correspondence regarding this application be sent to the firm of OBLON, SPIVAK, McCLELLAND, MAIER & NEUSTADT, P.C., whose post Office Address is Fourth Floor, 1755 Jefferson Davis Highway, Arlington, Virginia 22202.

We (I) declare that all statements made herein of our (my) own knowledge are true and that all statements made on information and belief are believed to be true ; and future that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such wilful false statements may jeopardise the validity of the application or any patent issuing thereon.

LEROUX Charles

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Signature of Inventor

July 09, 2001
Date

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